We claim:

1. An integrated circuit comprising:

an integrated circuit package having a first plurality of bonding pads;

a semiconductor substrate within the integrated circuit package and including a second plurality of bonding pads and having a surface area;

a plurality of wire bonds connecting selected ones of the first plurality of bonding pads to selected ones of the second plurality of bonding pads; and

an interconnection substrate mounted on the semiconductor substrate, the interconnection substrate having a surface area smaller than the semiconductor substrate surface area.

2. The integrated circuit of claim 1 wherein the interconnection substrate is flip chip bonded to the semiconductor substrate.

3. The integrated circuit of claim 1 wherein the interconnection substrate is formed from one of an organic material, ceramic, and silicon.

4. The integrated circuit of claim 1 wherein the interconnection substrate includes a conductive interconnect layer thereon.

5. The integrated circuit of claim 1 wherein the semiconductor substrate includes peripheral areas about the interconnect substrate and wherein at least some of the second plurality of bonding pads are within the peripheral areas.

6. The integrated circuit of claim 1 wherein the interconnection substrate further includes at least one filter capacitor.

7. The integrated circuit of claim 1 wherein the integrated circuit package includes a cavity and wherein the semiconductor substrate is adhered to the package within the cavity.

8. The integrated circuit of claim 1 wherein the integrated circuit package includes a substrate and wherein the first plurality of bond pads and the semiconductor substrate are carried by the integrated circuit package substrate.

9. An integrated circuit comprising:

an integrated circuit package having a first plurality of bonding pads;

a semiconductor substrate within the integrated circuit package and including a second plurality of bonding pads and having a surface area;

a plurality of wire bonds connecting selected ones of the first plurality of bonding pads to selected ones of the second plurality of bonding pads; and

an interconnection substrate flip chip mounted on the semiconductor substrate, the interconnection substrate having a surface area smaller than the semiconductor substrate surface area forming exposed peripheral areas in the semiconductor substrate and wherein

the second plurality of bonding pads are within the peripheral areas.

10. The integrated circuit of claim 9 wherein the interconnection substrate is formed from one of an organic material, ceramic, and silicon.

11. The integrated circuit of claim 9 wherein the interconnection substrate includes a conductive interconnect layer thereon.

12. The integrated circuit of claim 9 wherein the interconnection substrate further includes at least one filter capacitor.

13. The integrated circuit of claim 9 wherein the integrated circuit package includes a cavity and wherein the semiconductor substrate is adhered to the package within the cavity.

14. The integrated circuit of claim 9 wherein the integrated circuit package includes a substrate and wherein the first plurality of bond pads and the semiconductor substrate are carried by the integrated circuit package substrate.

15. An integrated circuit assembly comprising:

a semiconductor substrate including a plurality of bonding pads and having a surface area; and

an interconnection substrate flip chip mounted on the semiconductor substrate, the interconnection substrate having a surface area smaller than the semiconductor substrate surface area.

16. The integrated circuit assembly of claim 15 wherein the interconnection substrate is formed from one of an organic material, ceramic, and silicon.

17. The integrated circuit assembly of claim 15 wherein the interconnection substrate includes a conductive interconnect layer thereon.

18. The integrated circuit assembly of claim 15 wherein the semiconductor substrate includes peripheral areas about the interconnect substrate and wherein at least some of the plurality of bonding pads are within the peripheral areas.

19. The integrated circuit assembly of claim 15 further including at least one filter capacitor carried by the interconnection substrate.